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06CS33

Third Semester B.E. Degree Examination, December 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Table (1.1) shows a special code called gray code. For each gray there is a corresponding binary code. Design a code converter circuit which converts 4 bit gray code to a 4 bit binary code using only X – OR gates. **(12 Marks)**

A	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
B	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
C	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
D	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

Table 1.1

b. Implement the following equations using only three half adders [Note: using a single circuit]
i) $A \oplus B \oplus C$ ii) $\bar{A}BC + A\bar{B}C$ iii) $ABC + AB\bar{C}$ iv) ABC. **(04 Marks)**

c. Simplify the following equations using K – map.
i) $Y = F(A, B, C) = \sum m(1, 2, 3, 6, 7)$
ii) $Y = F(A, B, C, D) = \sum m(1, 2, 3, 6, 8, 9, 10, 12, 13, 14)$ **(04 Marks)**

2 a. A car safety alarm considers four inputs: Door closed (D), key in (K), seat pressure (S) and belt closed (B). The alarm (A) should sound if
* The key is in and the door is not closed (or) * The door is closed, the key is in, the driver is in the seat and the seat belt is not fastened.
i) Construct the truth table ii) Implement the above function using 8 : 1 MUX. **(06 Marks)**

b. Using a decoder and external gates, design the combinational circuit defined by the following three boolean functions.
i) $f1 = (\bar{y} + x)z$ ii) $f2 = \bar{y}\bar{z} + x\bar{y} + x\bar{z}$ iii) $f3 = (\bar{x} + y)z$. **(06 Marks)**

c. Design a 4 bit priority encoder, with D_0 having the highest priority and I/p D_3 the lowest priority. **(08 Marks)**

3 a. Explain the 4 bit adder – subtractor circuit, with an example. **(06 Marks)**

b. Show the 8 bit addition of these decimal numbers in 2'S complement representation.
i) + 89, – 34 ii) + 45, + 56. **(04 Marks)**

c. Explain carry look ahead adder. **(10 Marks)**

4 a. Derive the characteristic equation for JK flip flop and draw the state transition diagram for the same. **(06 Marks)**

b. Explain the Melay and Moore model of sequential circuit, with an example. **(06 Marks)**

c. A sequential circuit has two JK flip flops A and B, two inputs x and y and one output z. The flip flop I/P equations and circuit output equations are,

$J_A = Bx + \bar{B}\bar{y}$ $K_A = \bar{B}x\bar{y}$

$J_B = \bar{A}x$ $K_B = A + x\bar{y}$

$Z = A\bar{x}\bar{y} + B\bar{x}\bar{y}$

i) Draw the logic diagram ii) Tabulate the state analysis table
iii) Derive state equations for A and B. **(08 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – B

5 a. Explain the 4 bit programmable sequence detector and serial adder. **(10 Marks)**

b. Design a 3 bit binary up/down counter (synchronous) using T – flip flop. **(10 Marks)**

6 Design a sequential circuit which detects the given valid sequence, using D flip flop. Obtain the state diagram as well as state table.

The specification is as follows.

The sequential N/w having a single I/P line x, in which the symbols 0 and 1 are applied, and a single O/P line Z. An O/P of 1 is to be produced, coincident with the first 0 I/P symbol if it is followed exactly one or three 1 I/P symbols. All other times the N/w is to produce 0 output. Example sequence. **(20 Marks)**

x	0	1	0	0	0	1	1	0	1	1	1	0	1	0	1	1	1	1	0
y	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

7 a. Briefly discuss the Binary Ladders and explain 4 bit ladder. **(05 Marks)**

b. Explain the 4 – bit D/A converter, with a neat block diagram. **(08 Marks)**

c. Explain the 3 bit simultaneous A/D converter, with logic diagram, using 93/8 priority encoder. **(07 Marks)**

8 Explain in detail, all the TTL parameters. **(20 Marks)**

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